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(54) **A flat panel display and a process for its manufacture.**

(57) A flat panel VDU or TV screen (1) has pixel elements (P) controlled by an array of small single crystal semiconductor bars or chips (9). Power and information are connected directly or capacitatively to the chips (9); chip surfaces have pick-up pads (X', Y', D'). X-Y address lines (X,Y) are provided on a VDU panel substrate (3), and each chip (9) has bridging links (Y'Y') to complete continuity of the Y-line (Y). For data address, data lines (D) are provided on the substrate (3), and decoding and address recognition circuitry is incorporated in each chip (9). Chips (9) may be responsive to more than one address, and may be addressed either singly or a line or block at a time using a single code address. Each chip (9) may control its neighbouring pixels (8). A single crystal wafer (23) is processed and mounted upon a support (27). Chips (9) are defined by back etching the wafer and separated by stretching the support (27) prior to transfer to a substrate (5). Self aligned electrodes (X, Y, D) may be produced photolithographically, using shallow angle and overhead illumination. The chips or bars may also be located by means of vacuum chucks.

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A FLAT-PANEL DISPLAY AND A PROCESS FOR ITS MANUFACTURE

TECHNICAL FIELD

This invention relates to a flat-panel display and a process adapted for their manufacture. It is concerned particularly with electrically addressable panels for the display of graphics and information - video display units (VDUs), and also display screens for television (TV). More particularly, this invention concerns flat-panel displays of the type that incorporates semiconductor device components each of which serves to control and/or sustain the application of drive signal to a corresponding picture element (pixel) of the display.

BACKGROUND

Hitherto, construction of such flat-panel displays has been approached in one of two principal ways:-

The first approach uses a wafer of single crystal semiconductor material, usually silicon, as the rear electrode-bearing substrate of the display panel. The pixel control devices are integrated within this structure. Wrist-watch sized displays have been produced using this technique. Larger area panels using 20 cm diameter silicon wafers, are under current development. Even though this monolithic construction technology is well-advanced, there are drawbacks. The processing of 20 cm diameter wafers is both difficult and expensive because of problems relating to crystal uniformity, wafer warpage, wafer handling, etc. Also the area of silicon required is greater than that of the panel display area; a large quantity of semiconductor material is required. (See 'A 400 x 480 element dichrome display dye MOS LCD', K Kasahara et al, Society for Information Display XIV 1983. Library of Congress Card No 75-642555).

The second approach uses a thin film transistor technique; the rear substrate includes a film of polycrystalline or amorphous silicon in

which transistors are embodied. Difficulties arise due to the poor characteristics of devices made in polycrystalline silicon, especially as regards the leakage of reverse biassed pn junctions. Displays have been produced using this technique, typically displays with no more than 4×10^4 pixels, with most, but not all, pixels working. Much development will be required however, and many serious problems will need to be overcome, if working displays with 10^6 pixels are to be achieved. (See 'Silicon TFTs for Flat Panel Displays', F Morin, Proceedings of the 14th Conference (1982 International) on Solid State Devices, Tokyo 1980; Japanese Journal of Applied Physics 22 (1983) Supplement 22-1 pp481-485. Related articles by other authors follow on pp487-500).

THE DISCLOSURE OF THE INVENTION

The invention disclosed herein provides a flat-panel display of alternative construction to those outlined above.

In accordance with this invention there is provided a flat-panel display of the kind comprising electrode-bearing substrates, one each side of an electrically responsive optical medium, the electrodes born thereon being configured to define a multiplicity of pixels; together with, a multiplicity of electronic components for controlling the application of drive signals to pixel electrodes corresponding therewith;

characterised in that:-

said electronic components are embodied in physically separate elements of single-crystal semiconductor material, these elements being located between the electrode-bearing substrates and arranged with each element coupled to one or more neighbouring pixel electrodes.

The invention retains the advantages of using single-crystal material, but at the same time overcomes a disadvantage attendant hitherto, that

of processing an area of semiconductor material greater than that of the display area. Since the elements are of single crystal material, standard processing technology can be employed, and the components can be well characterised. The display offers the circuit complexity of a display mounted on single crystal silicon for displays with a much larger area and at a much lower cost because of the smaller chip area which need be processed. It can be used in either transmissive or reflective light modes, since the area of the elements need constitute but a small fraction of the total display area. Nor is it essential that the flat-panel display construction be planar. The flexibility of this approach allows construction over non-planar surfaces - eg over windscreens of cars or aircraft.

The flat-panel display may include bars of single-crystal semiconductor material, each bar extending over many adjacent pixel elements. Adjacent bars will be spaced apart in the direction normal to their extent. Whilst the length of such displays are limited to the size of wafer utilised for the purpose of construction, considerable lattitude is afforded in the orthogonal dimension.

Alternatively, the flat-panel display may include chips of single-crystal semiconductor material, these chips being arranged in a regular two-dimensional array. This allows a lattitude of choice for the length and width dimensions of the display. The chips may be of simple design, each overlapping only a single corresponding pixel electrode and serving to control only this electrode. However, with greater complexity in the integrated circuit design, and in the drive and address circuitry supporting the display, the chips may be arranged overlapping several adjacent pixel electrodes - eg 2, 4, or 6, and may control these several pixels simultaneously. With some sophistication, the chips may be made to incorporate quite complex circuits and may have considerable intelligence, so only changes of information updating the pictures need be sent to the display. The chips may also perform some processing of the picture - for example, they may scroll it or alter its contrast.

Provided that the thickness of each element - bar or chip - is chosen to match the thickness of the encapsulated medium - further advantage is attainable. Each element can thus serve as a spacer, assist in maintaining the thickness of the flat-panel uniform, and, add to panel rigidity - a feature particularly important in large area panels.

BRIEF INTRODUCTION OF THE DRAWINGS

In the drawings accompanying this specification:-

Figures 1 & 2: are illustrative drawings showing in plan, and in enlarged cross-section in plane I-I of this plan, respectively, part of a spaced-bar flat-panel liquid crystal display;

Figure 3: is a circuit diagram showing the construction of a typical pixel control circuit, one of many like circuits embodied in each of the bars shown in figures 1 & 2 above;

Figures 4 & 5: are illustrative drawings showing in plan, and in enlarged diagrammatic cross-section in plane II-II of this plan, respectively, part of an X-Y addressed distributed-chip flat-panel liquid crystal display, and showing circuit detail;

Figures 6A & B: are equivalent circuit diagrams for one of the Y-address lines of the display shown in figures 4 & 5 above, full equivalent and simplified equivalent circuits respectively. (Detail of boost amplification is omitted);

Figure 7: is a circuit and layout diagram, an alternative to the scheme of figure 5 above;

Figure 8: is a plan view of an electrode layout, to illustrate the use that can be made of parallel signal paths.

Figures 9 & 10: are illustrative drawings showing in plan and in enlarge cross-section in plane III-III of this plan, respectively, part of a data addressed chip element flat-panel display;

Figure 11: is a circuit diagram of a decoding circuit, one that can be incorporated within each chip for the display shown in figures 9 & 10 above;

Figure 12: is a timing diagram showing signals at points in the decoding circuit of figure 11;

Figure 13: is a schematic plan showing a possible encoder and chip layout such as may be used for a flat-panel TV-screen;

Figure 14: is an illustrative cross-section showing mounting of a grooved silicon wafer upon a elastomeric substrate, in preparation for chip separation;

Figures 15 & 16: are illustrative drawings showing in plan an in cross-section, respectively, chips, mask pattern and elastomer, as arranged prior to stretching;

Figures 17 & 18: are illustrative drawings in plan and cross-section, respectively, showing the same chips, mask pattern and elastomer, but after stretching;

Figures 19-21: illustrate the use of shadow techniques in the making of electrodes aligned to mounted chips,

Figures 22 & 23: are plan views of electrode structures produced by shadow techniques.

Figures 24a to 24d are sectional views of a vacuum chuck and chip array illustrating stages in a display manufacturing procedure,

Figure 25 schematically shows a plan view of four abutting chip wafers arranged for making displays with a vacuum chuck,

Figures 26a and 26b are schematic plan views of chip arrays before and after positioning on a display, and

Figure 27 is a schematic plan view of a chip array after one step in a procedure for positioning chips from a wafer on a display.

DESCRIPTION OF PREFERRED CONSTRUCTIONS

By way of example, a few embodiments of this invention will now be described.

Example 1

An X-Y multiplexed bar-element flat-panel display 1 is shown in figures 1 & 2. With reference to these figures and to figure 3, which shows a typical control circuit, this display 1 is seen to comprise electrode-bearing substrates 3, 5 spaced apart and arranged parallel to each other, each side of an encapsulated electrically-sensitive fluid optical medium 7, in this example a medium of liquid crystal material. One of the electrode structures, structure 3E on substrate 3, is subdivided into a large number of discrete square pixel electrodes PL,PR. The other electrode structure, structure 5E on substrate 5, is continuous. A number of elongate strips 9, bars of single-crystal silicon semiconductor material, have been arranged over the surface of the pixel electrodes. These strips lie parallel to each other and are spaced at twice the pixel pitch apart. Each strip 9 extends in the Y-direction and overlaps a fraction of the area of each of the pixel electrodes PL,PR lying adjacent to its sides. Each strip 9 is located between the substrates 3 & 5, and serves as a spacer. The upper surface of each bar 9 bears a metal coating 11. Good effective electrical contact is provided between this coating 11 and the continuous electrode structure 5E. A glue containing conductive particles, or a soft metal solder, 13, eg indium, serves to provide this contact. This is intended to provide effective earthing for the semiconductor bar 9. The lower surface of each bar 9 incorporates contact pads:- pads PL', PR' - for contacting the pixel electrodes PL PR, as also pads XL', XR' for contacting X-address electrodes XL,XR defined in the lower electrode structure 3E. Contact between these pads PL',PR',XL' & XR' and the corresponding substrate

electrodes PL,PR,XL & XR is made complete by soft metal solder, indium bumps 15. Each silicon bar 9 also encorporates a pair of drive lines D1, D2 together with a common Y-address line Y. Signals on the drive lines D1, D2 alternate each frame between positive and earth potential, and earth potential and negative, respectively. In the circuit shown in figure 3, the Y-line is connected to the gate of a first field-effect transistor T1. The source of this transistor T1 is connected to the X-address contact pad XR'. The drain of this transistor T1 is connected in parallel to the gates of two coupled transistors T2, T3 either complimentary p-channel/n-channel transistors or enhancement/depletion mode transistors operating in tandem. When a particular pixel is addressed, both the X-address and the Y-address go high once each frame. The drive signals alternate, and alternating potential is applied to the pixel electrode PR. It is arranged that the Y-address pulse ceases before the end of the X-address pulse so that charge is held on the gates of transistors T2 and T3. These transistors T2 and T3 are then held open for the duration of the frame, ie, until the next reversal of drive potential on lines D1, D2.

Typical dimensions

Silicon bars 100µm across on a 1mm pitch. Liquid crystal layer thickness 10µm. This construction affords considerable transparency and gives a factor ten reduction in the amount of processed silicon needed compared with a monolithic display of like dimensions. The silicon bars 9 may be positioned mechanically - for example by the techniques used to transfer chips to the tape in tape bonding. (See 'The Status of Tape Automated Bonding', T G O'Neal, Semiconductor International, February 1981, p33-51, & 'Microelectronic Packaging', G Sideris, McGraw Hill, 1968, p249). This is practicable because a typical display need only contain a few hundred bars. Alternative chip transfer procedures are described hereinafter.

Example 2

An X-Y multiplexed chip-element flat-panel display 1 is shown in figures 4 & 5. In this display the semiconductor elements 9 are in the form of chips and these have been distributed in a two-dimensional array arrangement to match the pixel electrodes P. Each chip 9 is dedicated to the control of a corresponding one of the pixel electrodes P, part of which it overlaps. X- and Y- matrix address lines X,Y are incorporated in the surface of the lower electrode bearing substrate 3. Alternating-current signal drive lines D are also provided on the substrate 3. These, as shown, are arranged parallel to the X-address lines X. Each chip 9 incorporates coupling pads X′,Y′, D′ & P′ to correspond to the address, drive and pixel electrodes X,Y,D&P. Accurate positioning of these pads X′,Y′,D′,&P′ relative to the underlying electrodes X,Y,D&P is a more difficult task than positioning in the previous example. For this reason, ac capacitative coupling rather than direct dc contact is tolerated within the constraints of design. A self-alignment technique is adopted to ensure reasonable accuracy in positioning. Details of alternative techniques are discussed later in this specification - see below.

A problem of this configuration is that the X- and Y-address lines X,Y are orthogonal and must cross. This may be overcome by using multi-level metallisation. In preference to this, however, bridging links at each cross-over may be built into the design of each chip. In this latter case, at typical address rates - eg 50 kHz - considerable loss is introduced in the interrupted lines, largely due to parasitic capacitance. This is illustrated by the equivalent circuit shown in figures 6A & B. Typical dimensions and impedance values are given below:-

R_t: Resistance of each section of Y-address line, each 1 mm long, 10 μm wide and 1 μm thick, aluminium material:- ~ 5Ω ;

R_L: Resistance of bridging links, each 200 μm long, 2μm wide and 1 μm thick:- ~ 5Ω ;

C_p: Pick-up capacitance, pad area 250 μm x 50 μm, dielectric spacing 0.1 μm, dielectric constant ε~3:- 3.3 pF ≡ 1MΩ @ 50MHz ;

C_e: Capacitance of line on chip to earth (back electrode 5E): area 200 μm x 2 μm, 1 μm spacing, dielectric constant ε~3:- 0.01pF;

C_t: Capacitance from track to top electrode: area 1 mm x 10 μm, 10 μm spacing, dielectric constant ε ~ 20: - 0.18pF.

The signal on the Y-line would decay by a factor $2C_t/Cp \simeq 11\%$ for each link. For this reason, boost amplification is provided by a non-inverting amplifier 15. As shown in figure 5, power for this amplification is derived by rectifying part of the ac drive signal - a rectifier 17 is connected between the drive pad D' and the earth electrode 5E. When both the X-address and Y-address are high the second transistor T2 conducts and connects the pixel electrode P' to the drive. Provided the Y-address pulse ceases before the end of the X-address pulse, the second transistor T2 will be held open for the remainder of the frame.

For a twisted nematic effect cell, a threshold voltage of about 2 volts is typical. For a dyed cholesteric-nematic phase change cell, a higher voltage of 10 volts is typical, for 10 μm layer thickness. In the design of the circuit, two conditions must be met. Firstly, the control transistor T2 (figure 5) must be able to turn the pixel on and off. Its impedance must be small compared with the series impedance in the drive signal path, when it is conducting. Its impedance must be large when it is non-conducting. This condition is readily satisfied:-

Transistor impedance:- ON: ~ kΩ ; OFF: ~ GΩ ;

Pixel capacitance (1 mm square, 10 μm spacing, ε =20): 90MΩ @ 100Hz;

Pick up and drive capacitance (2×10^{-8} m area, 0.1 μ spacing, ε=3): 30 MΩ each @ 100Hz

Drive line resistance:- ~ few kΩ.

Secondly, the pixel drive voltage must be sufficient to cause the liquid crystal material to change state, regardless of processing variations across the area of the display. It is indeed helpful that the liquid crystal switching is relatively sharp and that the application of larger signal than threshold has little appreciable effect albeit increasing power dissipation. This allows considerable lattitude. A 5V drive signal produces 5V across the pixel if the pick-up impedances and drive capacitances are near zero - ie if the pads and electrodes are in good touching contact. On the other hand, a spacing of 0.1 μm leads to a voltage of 3V across the pixel, and so is still somewhat in excess of the 2V minimum required to switch the pixel. This is well within the expected tolerance.

An alternative scheme, for boosting signal routed through the chips, is based on the circuit and layout of figure 7. This circuit relies on an additional line YY running parallel with each X-address line X. An extra coupling pad YY' is included in the chip 9. The line YY carries extra power for boosting the Y-address signal. Only one type of transistor is needed to implement this circuit.

In the circuits, thus far described, a number of faults can arise. The most serious are those that affect the tracks, since these can result in the loss of complete rows and/or columns of pixels. Such faults can arise as follows:-

1. Open and short circuit in tracks:- These can be avoided by testing the tracks before display assembly, followed by rejecting or repairing the electrode patterns as necessary. Parallel signal paths may be provided to reduce the incidence of catastrophic open circuit faults. This is especially important in the case of the bridged Y-address lines which are particulary vulnerable to this kind of fault. In the layout shown in figure 8, sections of the Y-address lines Y are extended in direction parallel to the X-address line X and Y-boost line YY so that they may be coupled to a pair of the chips 9. Connections within each chip 9 provide a continuous path, a bridging link, between broken parts of each Y-line Y. Provided that one or other of these links is made good, Y-signal will be propagated. The risk of interruption to the Y-lines is therefore reduced.

2. Pick-up electrodes on the chips - badly aligned to the substrate, and shorting the tracks:- Where the coupling is capacitive, as discussed above, this fault condition does not arise.

3. Faults on chip, short circuiting lines:- This only arises in the case of dc contact made between the chip pads and the lines. Protection may be afforded by including current limiting transistors in series with all transistor gates.

Faults, causing individual pixel failure, are also possible. These faults may be mitigated by circuit and layout duplication, or triplication. If capacitive coupling is adopted, parallel circuits, complete with coupling pads, can be embodied in each chip. Overall response thus will be an average. Circuit function can still result even in the event of one or some of these parallel circuits malfunctioning. The chips are all of the same design, so it is relatively easy to replace any chips that malfunction.

Example 3

A data-addressed chip-element flat-panel display 1 is shown in figures

9 and 10. Each chip 9 is arranged in a position where it overlaps four pixel electrodes P simultaneously. Each chip 9 incorporates four coupling pads P' which are arranged to couple capacitatively with the adjacent pixel electrodes P. The substrate electrode structure 3E also includes electrode tracks D, E and F running parallel in one direction between alternately adjacent pairs of the pixel electrodes, to carry drive signal, signal data including address information, and chip-to-chip data, respectively. Corresponding coupling pads D', E' and F' are incorporated in each chip 9. Coupling between pads D', E' and F' and the corresponding lines D, E, and F is capacitive.

The functions of circuits on the chips 9 can be broken down into four basic roles. Firstly, ac power from the coupling pads D' has to be rectified, smoothed and stablised so that it can be used to power the rest of the circuits. Secondly, ac data input signal eg frequency modulated signal as shown in figure 12, has to be converted into a chain of logic 1s and 0s voltage levels to which subsequent circuit logic can respond. As shown in figure 11 this part of the operation is performed using a pair of RC filters F1,F2 and a comparator CC. Each filter F1,F2 is designed with a different cut-off so the parallel pair can distinguish between frequency modulated pulses such as those shown in figure 12. When a pulse of the lower modulation frequency is applied to the pair of filters F1, F2, a logic 0 signal is produced at the comparator output. When a pulse of the higher modulation frequency is applied, a logic 1 signal results. Thirdly, the train of pulses has to be decoded. The train of binary digits thus produced are fed into a shift register S/R. Register transfer is controlled by a rectifier R, a smoothing filter F3 and a monostable M. The monstable M delays the register clock signal long enough to allow time for the binary signal to emerge from the comparator output, following the incidence of each modulated pulse. The register contents are relayed to the gates of a series of n-channel and p-channel field effect transistors which together provide a correlation filter. Coincidence is recognised when the logic 0,1 sequence is matched to the n & p channel sequence of the correlation filter. Once the chip recognises that it is being addressd, it feeds the succeeding bits of

data into a memory. Each chip may incorporate logic circuitry responsive to a number of different address codes. One code then may be used to address each chip individually. Other codes then may be used to address several chips simultaneously. Thus lines of pixels, or blocks or other patterns can be generated in response to a single code, making such pattern generation altogether faster. Chips may include several address recognition circuits in parallel for this purpose. Finally, this memory has to store data to indicate the state of the pixels controlled by the chip, and these pixels have to be driven at the correct frequency. An oscillator is required to drive the pixels and this may be provided by an astable, or by dividing down the timing signal frequency.

The frequency of the information and the power carrying signals is restricted by the RC time constants of the electrode tracks. It is difficult to reduce the track resistance below about 5kΩ/m or the capacitance below 200pF/m. The maximum frequency which can be employed on a section of track of length l (in metres) is therefore under $8 \times 10^4/l^2$Hz. The loading on the tracks from the circuits reduces this by a further factor 2 approx. The data rate must be an order of magnitude less than this. Thus if l≈0.3m, the maximum data rate is 4.0×10^4 bits/sec. Up to eight bits may be needed to announce the start of a packet of information, twenty to indicate which of 10^6 or so chips are being addressed and twelve to tell the chip what to do to update the four or so pixels under its control - forty bits in total. Thus a total of 10^3 chips (4×10^3 pixels) can be updated each second. This is adequate for a graphics VDU, but hardly suitable for TV application. However, there is no need to have just one encoder for the whole display; instead a number of encoders EE may be used in parallel, for example one to each line. Using lines 15 cm long and 150 chips per line (controlling 600 pixels), the pixels can be updated 25 times per second, clearly adequate for TV. The updating rate decreases rapidly as the screen size is made larger. For this reason it is desirable to drive the display from both sides, as is shown in figure 13, but even so it is likely to prove difficult to design TV screens more than 30 cm

(12") across.

Processing

Processing techniques for making displays of the invention will now be described with reference to figures 14 to 27. Chip circuits 21 may be made using a CMOS process on a silicon wafer 23 which has an etch stop layer 25 buried beneath its surface. Grooves are etched down to the etch stop 25 and the wafer 23 stuck face down onto the surface of an elastomeric sheet 27. Each chip 9 is fastened at one point 29 (figure 14). The wafer is then etched from the back to remove the bulk silicon and the etch stop layer 25. The chips 9 are then spread into an array by stretching the elastomer 27 (figures 15 to 18). The chips are then stuck down onto an electrode bearing substrate 5 and the elastomer sheet 27 removed. A second electrode bearing substrate 3 acts as the lower substrate of the panel 1. A metallisation pattern is made on this substrate to provide pixel electrodes, power lines, etc. Since there may be slight non-uniformities in the stretching of the elastomer 27, it is necessary to ensure that this pattern is aligned with the chips 9 at all points. This can be achieved by placing a mask pattern 31 on the elastomeric substrate which would be stretched together with the chips 9. A photolithographic process is then used using the mask pattern to define the electrode pattern on the lower face of the display panel. Alternatively, the array of chips 9 on the upper substrate 5 can be illuminated at a shallow angle and the shadows cast can be used to photolithographically produce a matching electrode pattern (figures 19 to 23). The substrates 3 and 5 are then placed together, the panel filled with liquid crystal material 7 and sealed.

The process may be carried out by steps (1) to (15) set out below:

1. Grow 10 μm of epitaxial silicon on top of a p++ or buried oxide layer 25. This buried layer will later act as an etch stop. A buried oxide layer may be produced under silicon by ion implantation, silicon

anodisation or by recrystallisation of polysilicon deposited on oxide. Silicon may be anodised in hydrofluoric acid. If appropriately doped silicon is used, silicon structures separated from the bulk by a porous film can be produced. In all cases the silicon layer may be thickened by further epitaxial deposition.

2. Make integrated circuits 21 using eg a standard CMOS process.

3. Cover the circuits 21 with a passivation layer 33 eg a layer of nitride. (This may be produced by sputtering, plasma assisted chemical vapour deposition or, if metallisation on the chips is polysilicon or silicide, by chemical vapour deposition).

4. Pattern the passivation layer 33 and etch down to the etch stop 25 using plasma or an anisotropic etchant, eg ethylene diamine pyrocatechol or aqueous potassium hydroxide, using the patterned passivation layer 33 as a mask.

5. Put globules of material 29, eg, photoresist, 1 μm high and 3 μm in diameter, at a given point on each chip 9. Preferably this is close to one corner of the chip.

6. Place the structure face down onto the surface of a glue-coated planar elastomeric sheet 27. The globules 29 serve to ensure single point contact between each chip 9 and the sheet 27. The configuration is shown in figure 14. The best elastomer thus far identified is amorphous polyethylene terapthalate (PET), a material manufactured by ICI Plastics Division, England. This material stretches uniformly on both a microscopic and macroscopic scale at 80C and yet is rigid at room temperature. It is also inexpensive, non-contaminating (it contains only carbon, hydrogen and oxygen) and is resistant to chemical attack.

7. Mount the elastomer sheet 27 in a holder and etch the silicon array from the back of the wafer 23, until the etch stop 25 is reached.

8. Remove the etch stop layer 25 to separate the individual silicon chips 9. In the case of oxide as etch stop layer 25, this may be performed using buffered hydrofluoric acid. Alternatively the etch stop layer 25 may be removed by plasma etching or by ion beam milling.

9. If necessary, wash carefully and dry.

10. Apply a metal coating to the back surface of the chips 9 by evaporation at a shallow angle to avoid filling in grooves or coating the elastomer (See figures 15 and 16).

11. Stretch the elastomeric sheet 27 slowly by a factor 4 in each direction. This may be performed using a large number of clamps about the periphery of the sheet 27. (See figures 17 and 18). Alternatively the sheet can be clamped and expanded by hydrostatic pressure. The shape of the expanded elastomer can be determined by means of a mould.

12. Lower onto the electrode bearing substrate 5 and affix. The continuous electrode structure 5E on this substrate 5 serves as earth electrode for the panel. A conductive adhesive agent is used. Since in general conductive glues and solders are opaque, surplus material is removed. This may be achieved by coating the substrate 5 with a suitable agent, eg indium metal, covering with photoresist, using the chips as a contact mask, illuminating, developing the photoresist, dissolving away the exposed agent and removing the remaining photoresist, leaving pads of glue or solder corresponding in size and position to the chips 9. Alternatively, the chips can be located on the adhesive agent and used as masks to protect this agent during removal of surplus material so that adhesive agent remains only beneath the chips.

13. Remove the resist globules 29. This may be done using acetone as solvent. The elastomeric sheet 27 is then removed.

14. The substate 3 which is to be used to form the other face of the display panel 1 must be patterned so as to produce power and data lines and the pixel control electrodes P of the display. The power and data lines must be of low resistivity and must be of a good metallic conductor eg aluminium. The liquid crystal pixel control electrodes can be of either metal or a transparent conductor, eg, cadmium stannate or indium tin oxide. In either case the pattern must be aligned to the actual distribution of the chips 9 since it is unlikely that the stretching will be accurate enough to allow use of non self-aligned technique. The may be achieved in two ways:-

(i) The first is to lay down a pattern on the elastomeric sheet before it is stuck to the wafer in step (6). This pattern would be made of a material which would stretch with the elastomer, eg resist or rubber. It would correspond to the pattern of electrodes which is eventually required and would be aligned with the wafer. After the elastomer has been stretched and the chips removed, the pattern can be used to produce a photomask to pattern the lower electrode 3E of the display.

The material of which the pattern is made is not usually very opaque, so it will not furnish a mask directly. One way of getting round this is to deposit a thin layer of metal on the pattern after the elastomer has been stretched. The metal can then be patterned by liftoff. The resulting metal pattern can then be used to make a mask which in turn can be used to photolithographically define the electrode pattern 3E on the lower substrate 3. This two step process is needed because each step produces inversion of the image. By going through two steps the original pattern is regained so that the pattern on the lower substrate 3 is a faithful copy of that on the elastomeric sheet. By choosing the photographic process, and the process used for producing the electrode pattern on the lower substrate 3 to be direct or reversal processes, the pattern produced on the lower substrate 3 can be made either the same as or the reverse of that on the elastomeric sheet 27. For example, if the elastomeric sheet 27 has a resist pattern 31 on it which is the same as that illustrated in figure 15

(before stretching) or figure 17 (after stretching), and liftoff is used, then the metal pattern on the elastomer becomes similar to that desired for the electrode pattern on the lower substrate 3, as shown in figure 9. If the photographic process used for making the mask is a reversal process , and so is the process by which the pattern on the mask is transferred to make the electrode pattern on the lower substrate, the electrode pattern of figure 9 is produced on the lower substrate. Messy lift off may be avoided if the pattern is made either using a dye (eg procinyl red G) on the elastomer, or using a dye-containing material. An opaque pattern could then be made directly. If the dye pattern consisted of two layers containing dyes which absorb at different wavelengths, then it could effectively contain two different patterns, both aligned with the chips. The result which is produced when the elastomer is used as a lithography mask would depend on the wavelength of the light used. This would make it possible to produce metallisation patterns of two different materials eg aluminium for power lines and indium tin oxide for the pixel control elements, both aligned to the chip pattern. If a dye were in the resist, the resist would have to be patterned at a wavelength at which the dye did not absorb.

(ii) The second method is to use the substrate 5 with the chips 9 on as a shadow mask which can be used to define a matching electrode pattern 35 on the lower substrate 3. The process is illustrated in figure 19. In order to avoid diffraction problems it is best if the chips are actually resting on resist 35. Shadows 37 produced are clearly much too large to form useful features, but provided the mounted chips are displaced sideways and another exposure is performed, much thinner features 39 can be produced (figure 20). After each photolith the patterned metallisation 3E is passivated before the next step, eg by anodisation or by deposition of a dielectric such as silicon dioxide.

It is straightforward to build up the regular pattern in the display itself, but one problem is to make correct connections to the ends of the power and address lines. This can be achieved by a combination of

two techniques. Firstly, chips 9 at the ends of rows are chosen to be wider than those elsewhere and the chips 9,9' raised above the lower substrate 3, eg by the insertion of a glass plate between the chips 9 and the lower substrate 3. More than one light source is used. Full shadow is produced only by the larger chips 9' (figure 21). Secondly, it is possible to make one set of address lines with shadows going one way and one set with the shadows going in the opposite direction so the contacts to the two sets of lines extend out of the array in different directions (figure 22). Using these two techniques it is quite possible to make a structure of the type illustrated in figure 23. Electrodes D are produced by the technique of figure 19. Electrodes DD are produced by shifting the chips 9 sideways making one exposure, using the technique of figure 21, then shifting the chips sideways in the opposite direction and making another exposure.

The latter technique (ii) has the advantage that some features can be made using one type of metallisation and others using a different type, but the former technique (i) is simpler and less expensive and is therefore to be preferred.

15. Stick down the chips 9 and top substrate 5 to the bottom substrate 3 and fill with liquid crystal material7.

Referring now to figures 24a to 24d, there is illustrated in section apparatus for a further process for mounting integrated circuit chips in a flat-panel display. A wafer (not shown) is attached releasably to a surface 40 and divided to form a two-dimensional array of chips such as 9 with solder bumps 15 as previously described, one row of the array of chips being shown. As shown in figure 24a, a vacuum chuck 41 is positioned over the chips 9. The chuck 41 has holes such as 43 spaced appropriately for location adjacent every third chip 9. As shown in figure 24b, an inner region 45 of the chuck 41 is evacuated; every third chip 9 is lifted by the chuck 41 and thereby released from the surface 40. The released chips 9 are transferred to an electrode-bearing display substrate 3. A heater 47 is employed to melt the solder bumps 15 attaching the chips 9 to the substrate 3. Finally, as shown in figure 24d, the chuck vacuum is released and the chuck 41 removed. These operations may be repeated as required to deposit a larger number of chips. Figures 24a to 24d show every third chip 9 being positioned. By repositioning the chuck between each cycle of operations and carrying out three cycles, all chips may be transferred to the display.

The vacuum chuck may be made by engineering techniques. Because chips are a few hundred microns across, machining holes of the appropriate size and spacing is not straightforward. It is preferred to employ a chuck with a silicon surface perforated by anisotropic etching. A 100 orientation silicon wafer is polished on both faces and a 1 μm oxide layer is grown thereon. Holes are etched in one oxide layer face by conventional photolithographic masking techniques. The wafer is then etched anisotropically with an etchant which attacks 111 planes far more slowly than other planes, eg EDA, solutions of potassium hydroxide in water or water-alcohol mixtures. These procedures are

described in Proc IEEE 70 (5) pp 420-457, May 1982, K E Peterson. The silicon wafer is etched back until 111 planes are reached, and etching virtually ceases. This produces holes through the silicon defined by 111 crystal planes. The residual oxide layer is removed with 5:1 ammonium fluoride: hydrofluoric acid to produce a perforated silicon plate.

The perforated silicon plate may be provided with a backing support, such as a metal element with drill holes providing vacuum communication to the perforations. Either the silicon plate or the backing support is grooved so that vacuum communication is arranged via the holes in the support, the grooves and finally the silicon plate perforations. This reduces the precision necessary in drilling holes in the support.

Referring now to figure 25, there is shown a square array of four abutting wafers 50_1 to 50_4 arranged for application of chips to a display larger in extent than one wafer. Each wafer 50 is a square array of sixty-four chips of four different respective kinds. Each chip is indicated by a square such as 52. The wafers 50_1 to 50_4 provide a total of sixteen kinds of chips. Each chip kind is located in a respective quarter section of a respective wafer. For example, the sixteen chips adjacent the reference (0,0) in figure 25 form the upper left quarter of wafer 50_1. References (m,n) (m,n = 0,1,2 or 3) in the figure both identify the sixteen different kinds of chip 52 and indicate the chip position on a display substrate. First reference m indicates the mth display column and second reference n the nth display column.

The chips are separated from one another in the wafers 50 as previously described. A vacuum chuck large enough to cover all four wafers is employed to transfer one chip of each kind to a display.

The chuck has a hole spacing equal to the distance between centres of four collinear chips. The holes form a two-dimensional array, and the chuck transfers one chip from each wafer quarter section to produce one display substrate. The chuck is then repositioned to transfer successive sets of different chips to successive substrates. This procedure is useful inter alia in forming a display incorporating chips which have different prearranged address codes.

Referring now to figures 26a and 26b, there are shown chip layouts 60 and 61 respectively before and after positioning on a display substrate (not shown) in a four stage transfer procedure. Chip layout 60 corresponds to a wafer divided into individual chips as previously described. Each chip such as 62 is labelled with column and row indices (m,n), where m,n = 0 to 7, these indicating positions on the display substrate.

Chips 62 in layout 60 have one of four forms of shading, rightward oblique, leftward oblique, dotted or clear. The arrangement is such that any four adjacent chips all differ in shading. Moreover, chips of like shading are spaced appropriately for location in a respective quarter section of layout 61 in which chip shading corresponds. A vacuum chuck is employed having a 4 x 4 square array of suction holes with a centre spacing equal to that between alternate chip centres. This enables the chuck to raise all chips of one respective shading in one transfer step. Initially, the chuck is employed to raise all chips with rightward oblique shading. These are then transferred to the upper left quarter 63 of display layout 61. On three subsequent transfer stages, the chips with leftward oblique shading, dots and no shading are transferred respectively to the upper right, lower left and lower right quarters 64, 65 and 66 of display layout 61.

When a large number of transfer operations is required in operations using the immediately foregoing procedure, an alternative approach may be adopted. Referring now also to figure 27, the chip layout 60 of figure 26a could be repositioned into the spaced column array 70 in a first step. This would require a first vacuum chuck arranged to raise alternate columns of chips. A second chuck would then be employed to reposition alternate chips in each column, recreating the figure 26b display layout 61. The advantages of this become apparent if the spacing of the chips on the display substrate is to be four times the chip dimensions in both X and Y directions. The figure 26 approach requires sixteen transfer steps with one chuck, but that of figure 27 eight steps with two chucks.

Chip or bar positioning on a display substrate may also be carried out by the use of a "pick and place" machine. This may be appropriate for positioning comparatively few elements, eg an array of silicon bar elements.

CLAIMS

1. A flat-panel display of the kind having an electrically responsive optical medium arranged between electrode-bearing substrates, the electrodes being configured to define a multiplicity of pixels, together with a multiplicity of electronic components for controlling the application of drive signals to pixel electrodes corresponding therewith,

characterised in that:-

the said electronic components are physically separate elements of single-crystal semiconductor material, are located between the electrode-bearing substrates and are arranged with each element coupled to at least one neighbouring pixel electrode.

2. A display as claimed in claim 1 characterised in that the elements of single crystal material are bars.

3. A display as claimed in claim 3 characterised in that the elements of single crystal are chips.

4. A display as claimed in claim 3 characterised in that each chip overlaps and is coupled to a plurality of pixel control electrodes each of which it serves to control.

5. A display as claimed in any one of the preceding claims characterised in that the elements serve as structural spacers between the electrode bearing substrates.

6. A display as claimed in any one of the preceding claims characterised in that electrodes of one of the substrates are coupled capacitively to the semiconductor elements.

7. A display as claimed in any one of the preceding claims, being an X-Y matrix addressed display, characterised in that one of the electrode bearing substrates has pixel control electrodes and also electrodes for X & Y address.

8. A display as claimed in claim 7 characterised in that it comprises chip elements each including a bridging link to complete continuity of a corresponding address electrode.

9. A display as claimed in claim 8 characterised in that the bridging link includes a boost amplifier.

10. A display as claimed in claim 8 or 9 characterised in that each X or Y address electrode is coupled to one row (or column) of chips and also to the next adjacent row (or column) of chips, a bridging link being included in each pair of the adjacent chips to provide an alternative path for continuity.

11. A display as claimed in any one of the preceding claims 1 to 6, being a data addressed display, characterised in that one of the electrode bearing substrates has pixel control electrodes and also electrodes for data address, and each semiconductor element includes circuitry for address recognition.

12. A display as claimed in claim 11 characterised in that each element is responsive to a frequency or pulse code modulated address.

13. A display as claimed in claim 11 or 12 characterised in that each element is a chip responsive to more than a single address, and a plurality of the chips have at least one address in common such that a line, block or pattern of chips can respond simultaneously to a single address.

14. A display as claimed in any one of the preceding claims 11 to 13 characterised in that it includes coupling between adjacent elements for the transfer of data from element to element.

15. A display as claimed in any one of the preceding claims 11 to 14 characterised in that each element is a chip, the chips are arranged in rows and each row has an encoder for addressing the chips therein.

16. A display as claimed in claim 15 characterised in that each row has a pair of encoders, one at each end of the row.

17. A display as claimed in any one of the preceding claims, characterised in that each element includes duplicate circuits and pick-up electrode pads for performing the same function.

18. A display as claimed in any one of the preceding claims, characterised in that each element includes circuitry responsive to address signal or to pixel drive signal for extracting power therefrom to operate other circuitry incorporated therein.

19. A method, for producing the display as claimed in claim 1, characterised in that it includes the following steps:-

forming a multiplicity of like circuits in the surface of a semiconductor wafer; forming a passiviation layer over the wafer surface; forming grooves in the wafer to isolate the like circuits, these grooves extending to a depth reaching an etch stop layer buried in the wafer;

removing bulk semiconductor material from the reverse side of the wafer; and,

removing the etch stop layer to separate the like circuits to form a multiplicity of semiconductor elements.

20. A method according to claim 19 characterised in that it includes the further step of transferring the separated circuits to a supporting substrate with the aid of a vacuum chuck.

21. A method according to claim 20 characterised in that the vacuum chuck has a suction surface of perforated silicon.

22. A method as claimed in claim 19 characterised in that it includes the following additional steps:-

prior to separating the like circuits, mounting the wafer face down on an elastomeric support,
subsequent to separating the like circuits, stretching the elastomeric support to space out the circuits, and
transferring the circuits to a supporting substrate.

23. A method as claimed in any one of claims 19 to 22 characterised in that the circuits are bonded to the supporting substrate by an electrically conductive adhesive agent, the circuits being used as a protective mask during removal of surplus adhesive agent.

24. A method as claimed in claim 22 characterised in that the surface of the elastomeric support has a mask pattern thereon, the wafer is mounted on the support so that it lies over the mask pattern and the mask pattern is subsequently enlarged with stretching of the elastomeric support for use thereafter as a mask for defining electrodes.

25. A method as claimed in claim 22 or 24, wherein the transferred circuits are used in defining electrodes aligned therewith, the following steps being performed:-

providing a metallised substrate having a photoresist coating;

locating the transferred circuits over and in contact with the coated substrate;

illuminating the transferred circuits at a shallow angle to form a continuous shadow;

inching the transferred circuits sideways;

illuminating the transferred circuits a second time to form another continuous shadow;

developing the photoresist to define an area corresponding to the area of common shadow; and

defining the electrodes using the patterned photoresist as an etch resistant mask.

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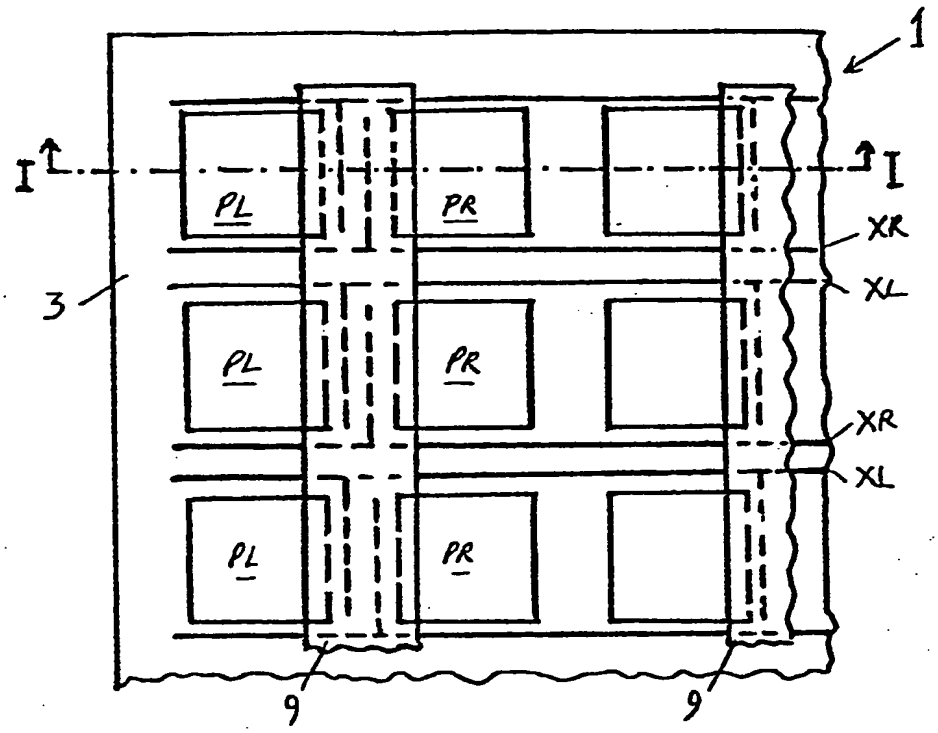

FIG. 1

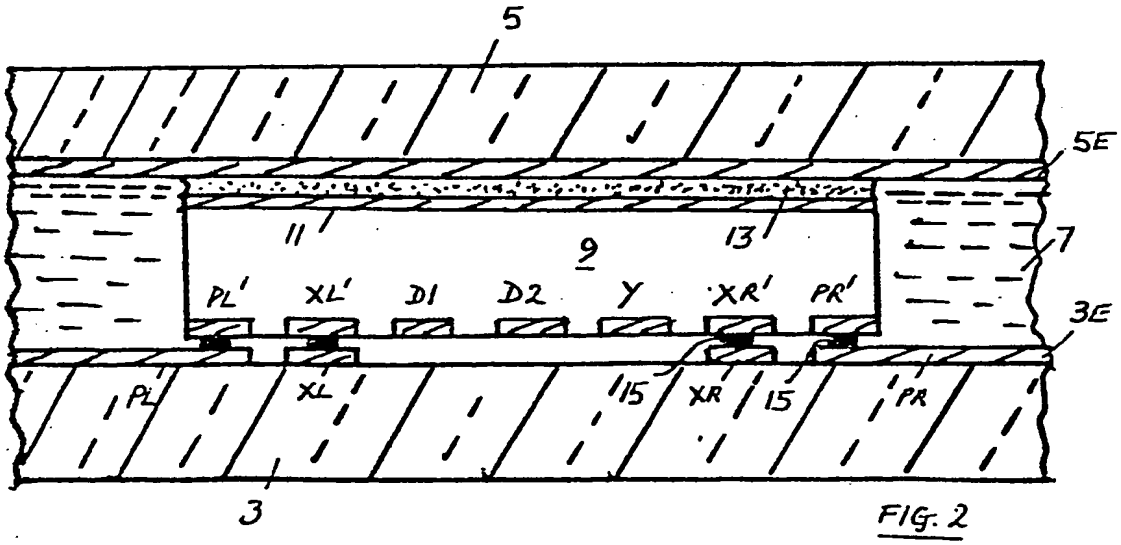

FIG. 2

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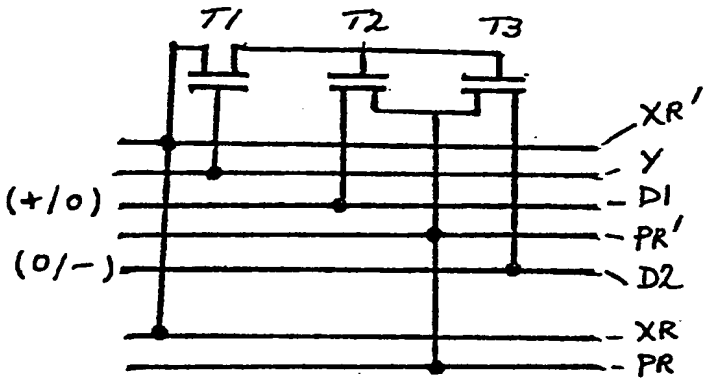

FIG.3

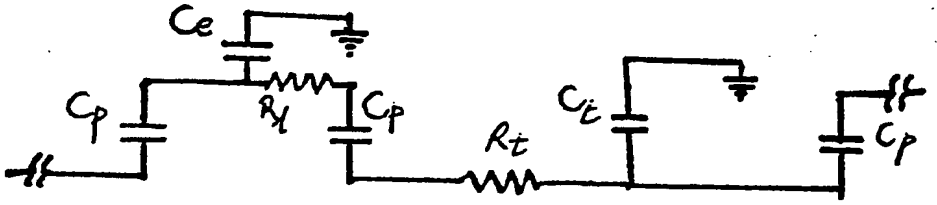

FIG. 6A

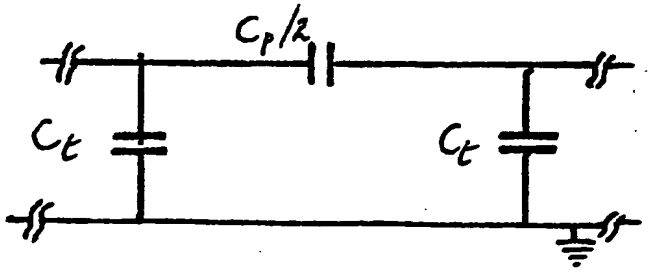

FIG. 6B

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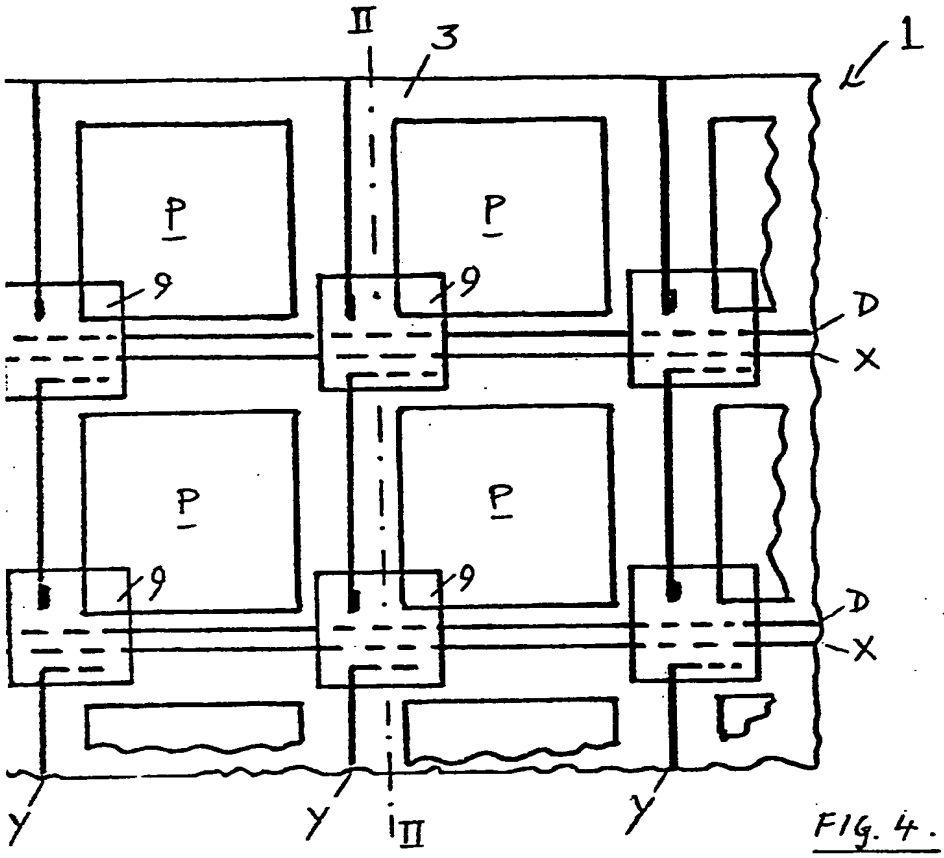

FIG. 4.

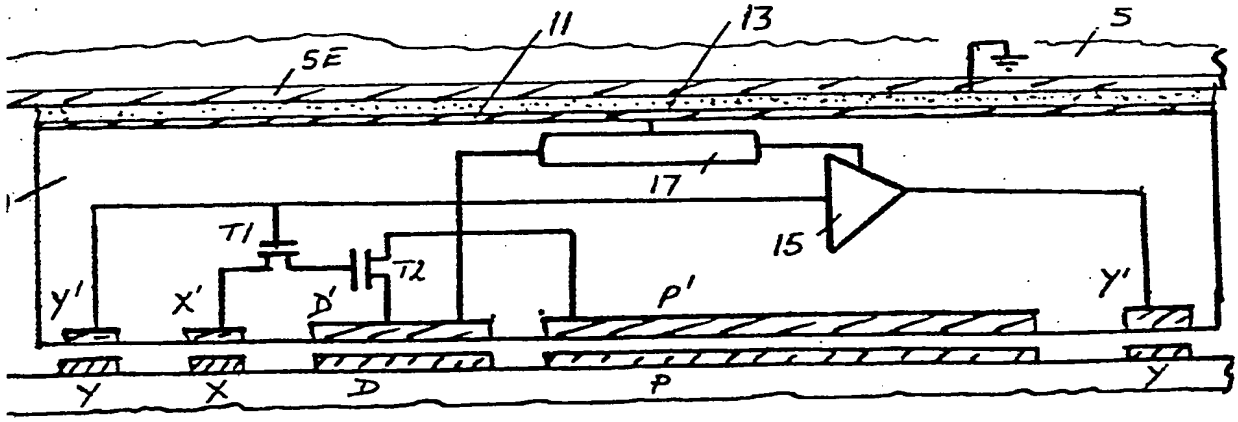

FIG 5

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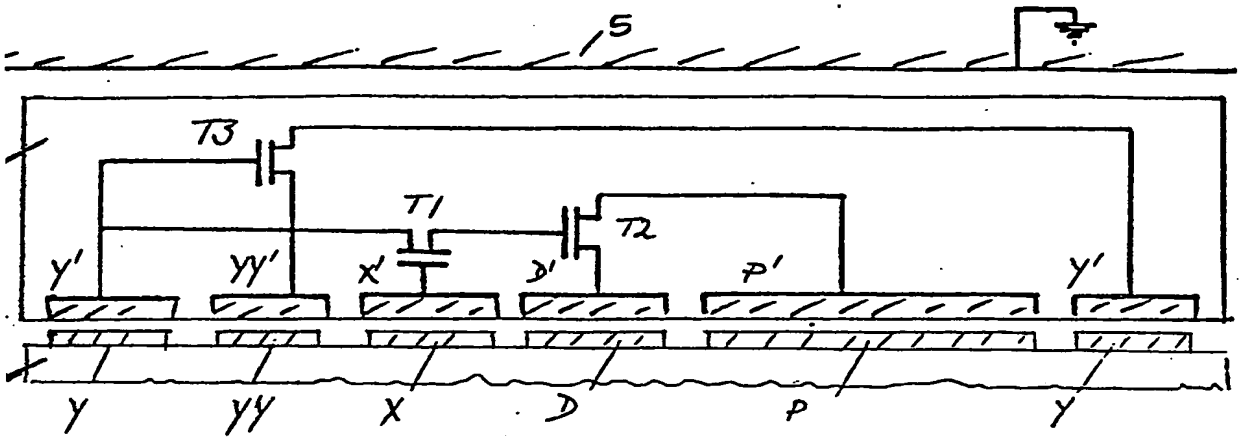

FIG. 7

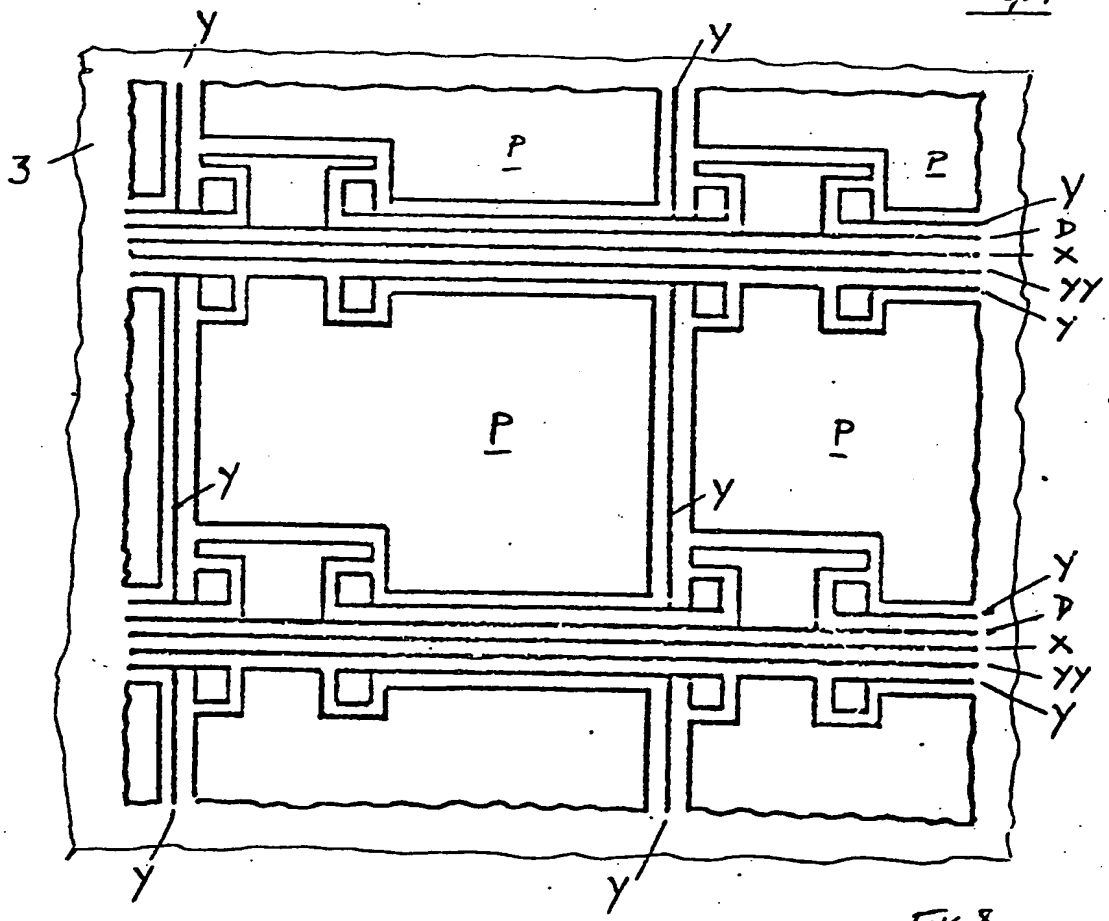

Fig. 8

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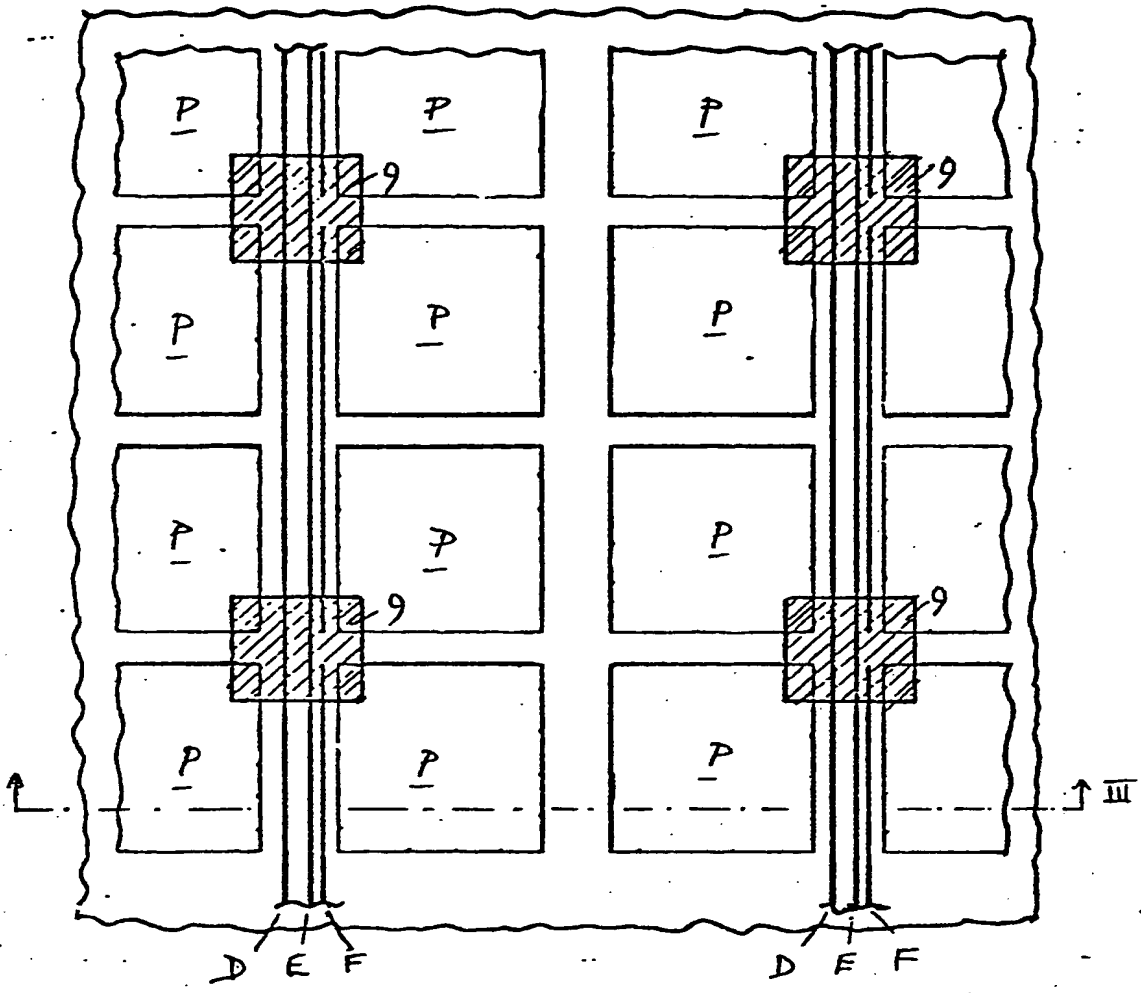

Fig 9

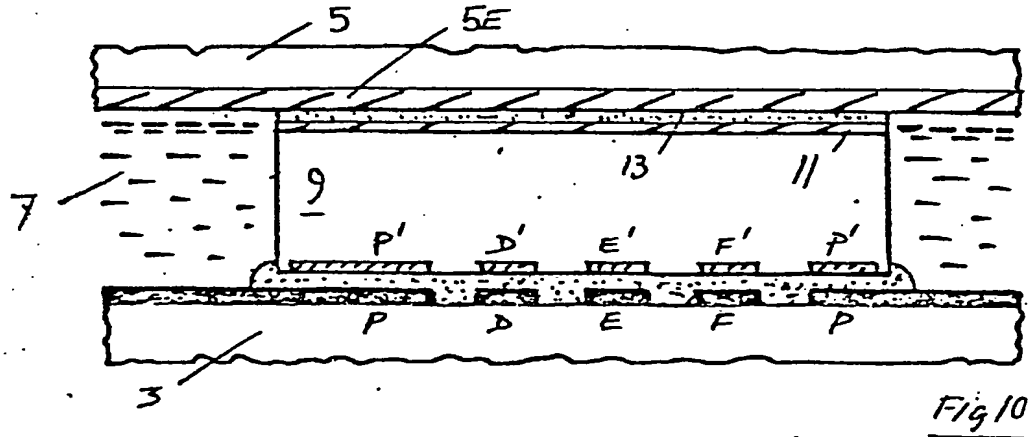

Fig 10

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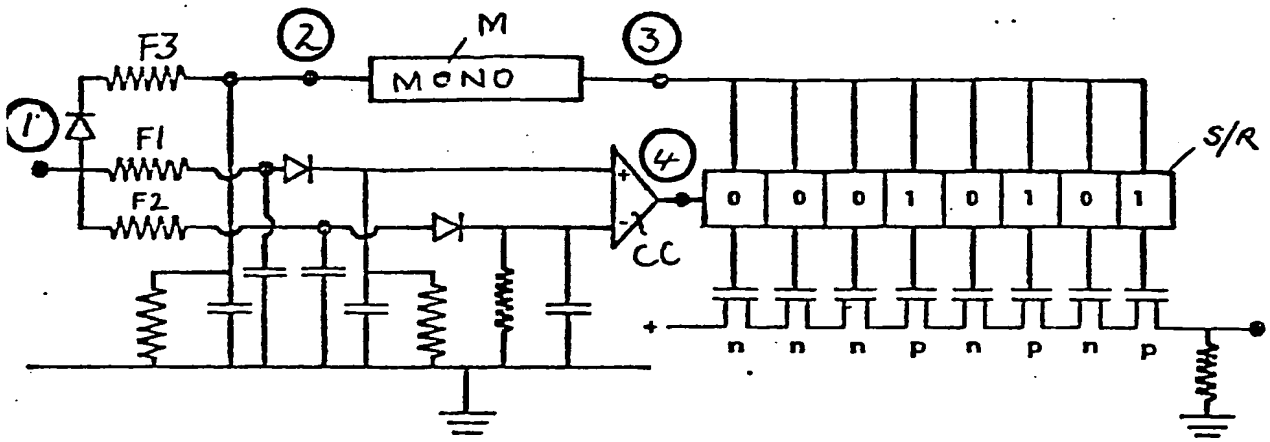

FIG. 11

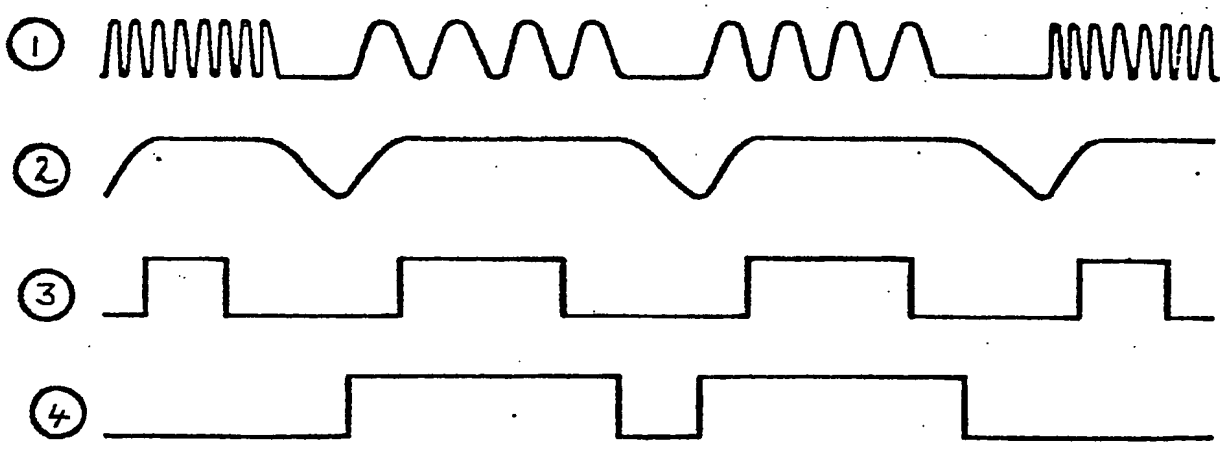

FIG. 12

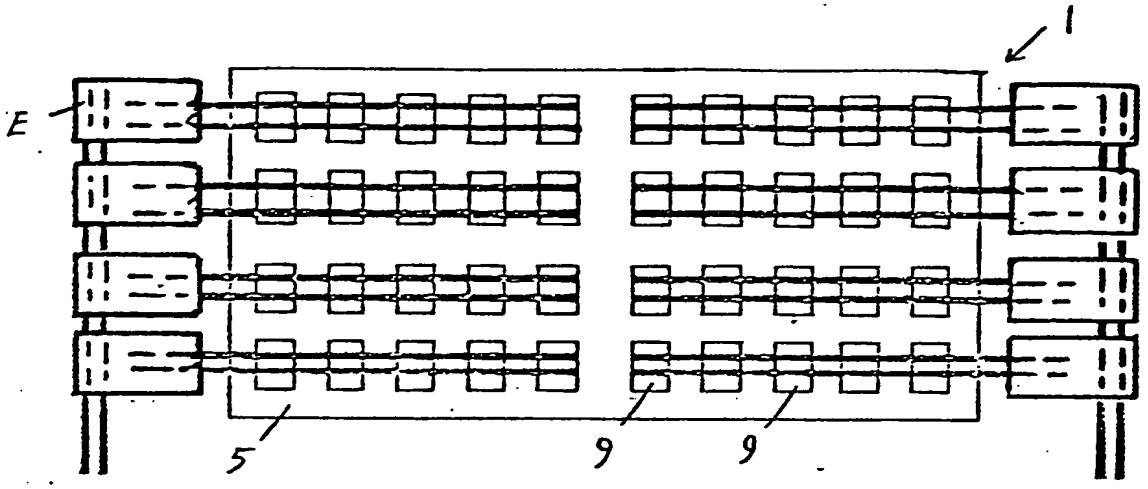

FIG. 13

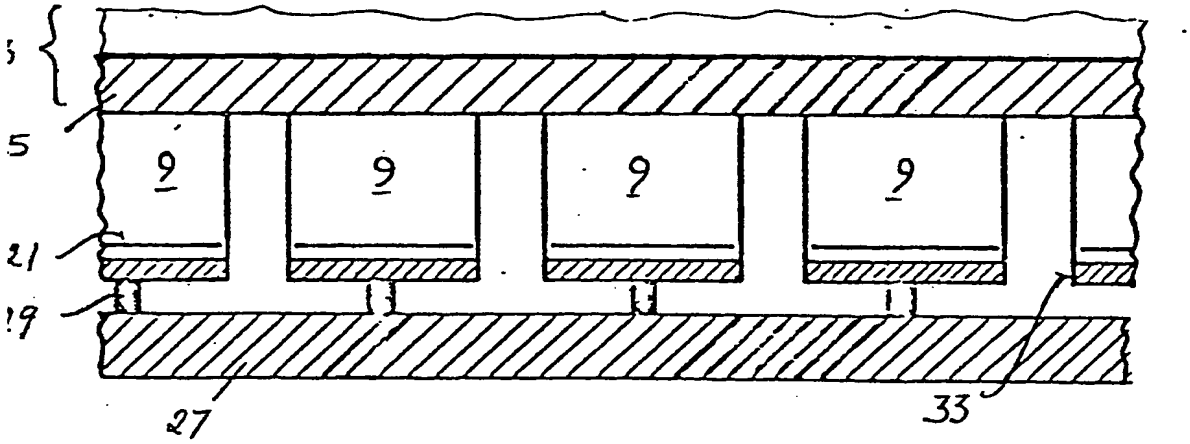

FIG. 14

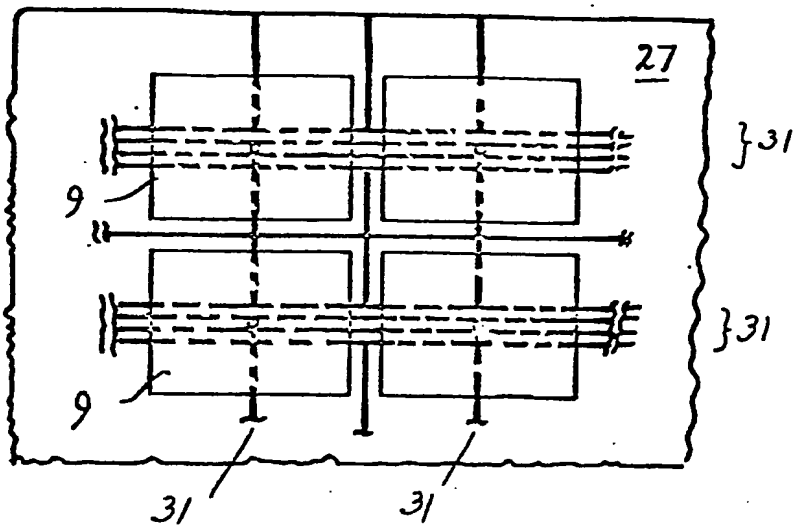

FIG. 15

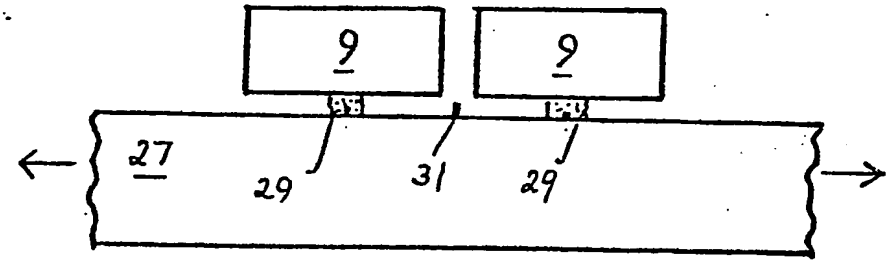

FIG. 16

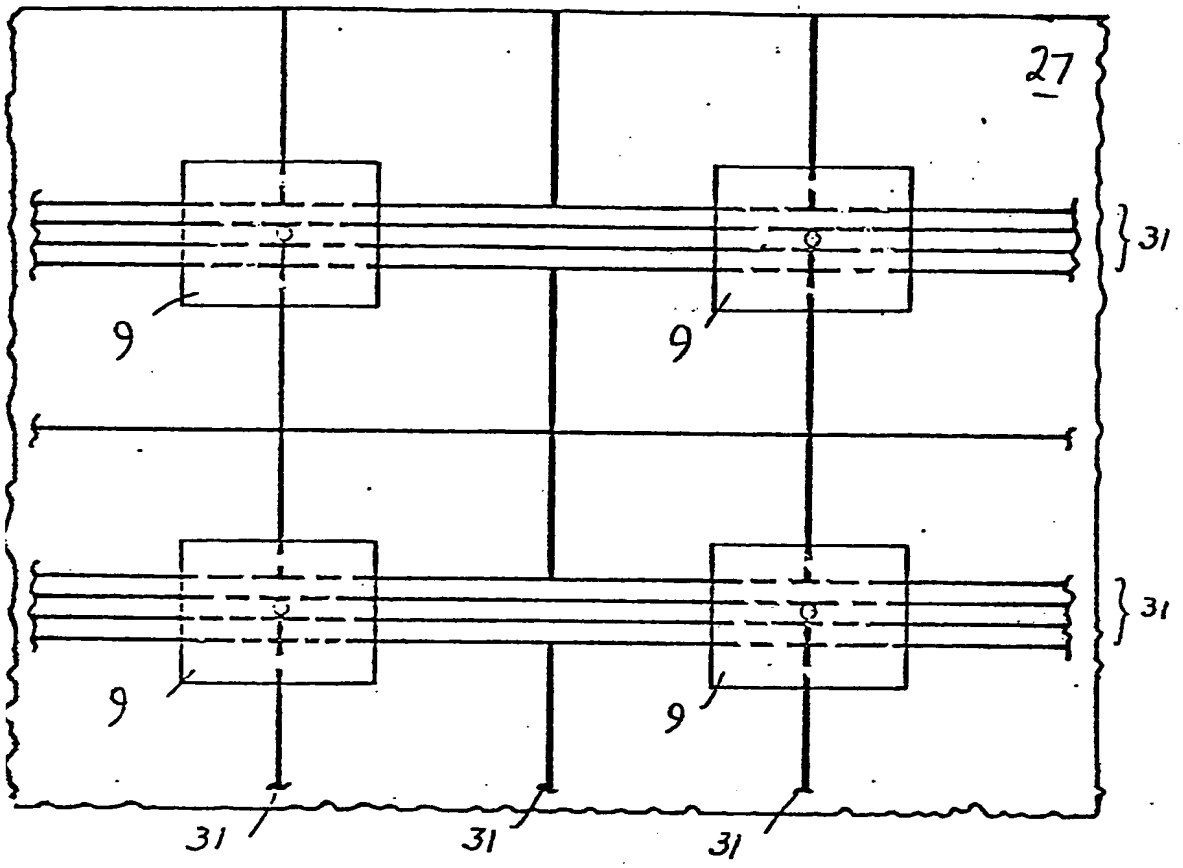

FIG. 17

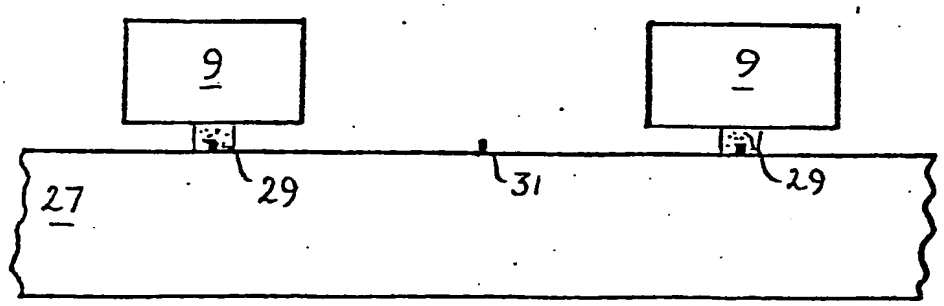

FIG. 18

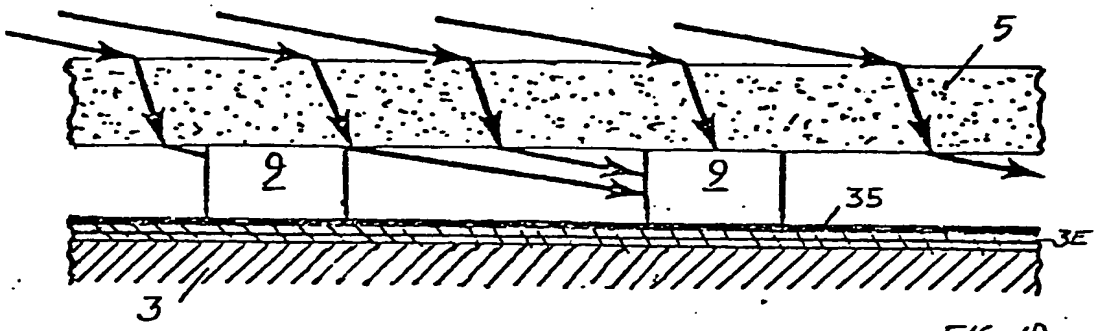

FIG. 19

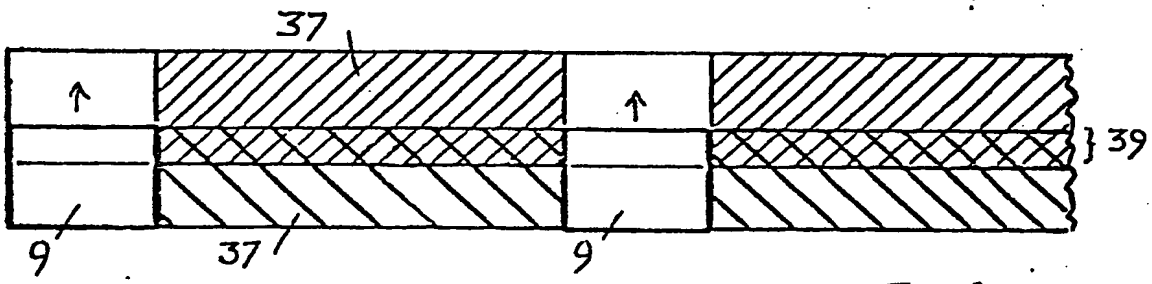

FIG. 20

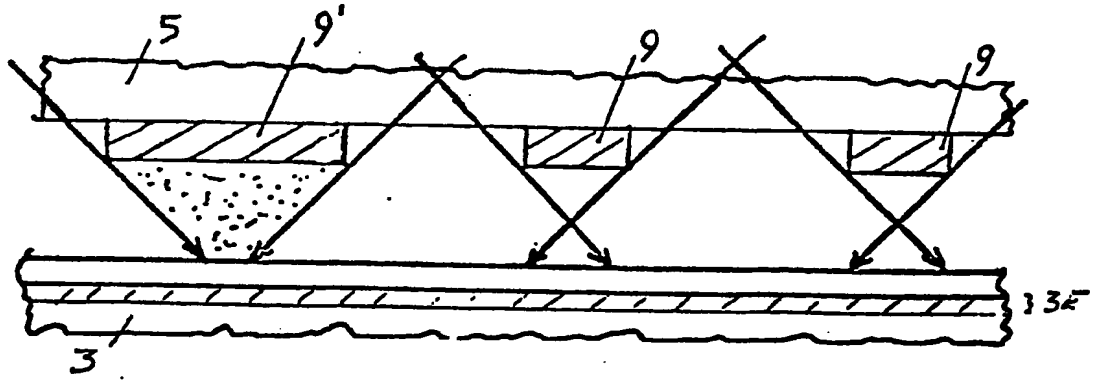

FIG. 21

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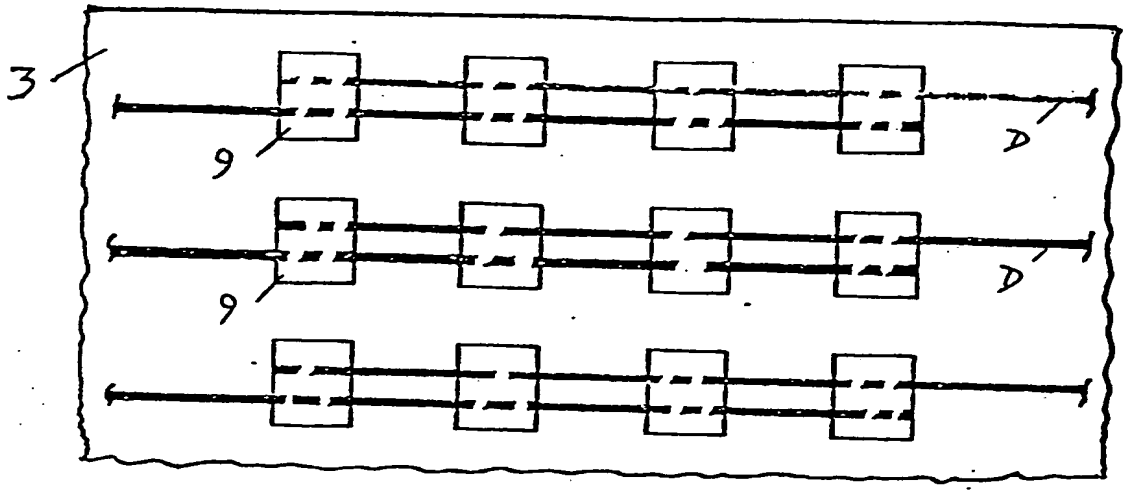

FIG. 22

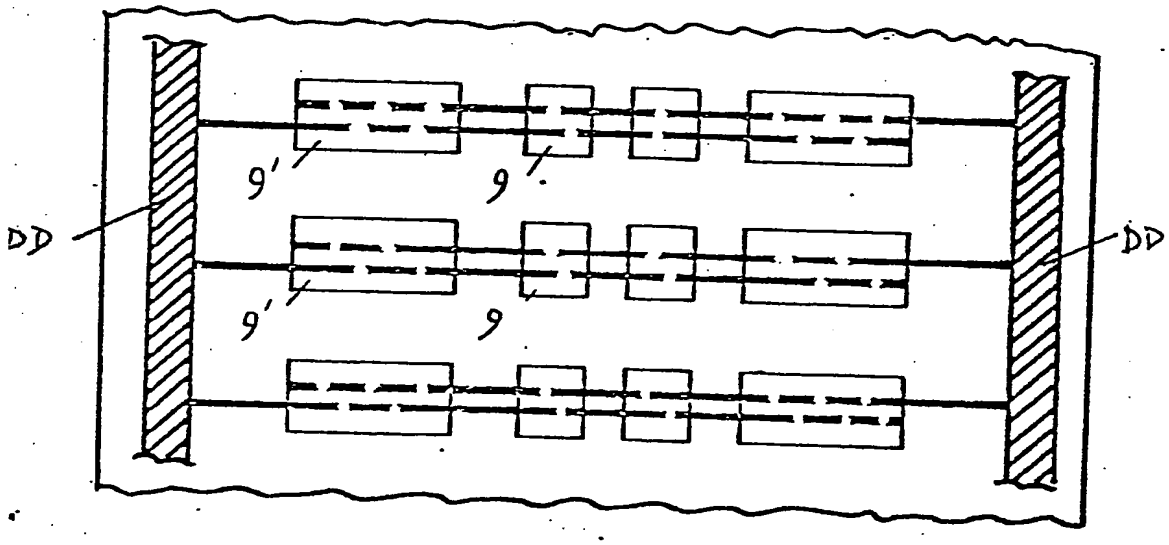

FIG. 23

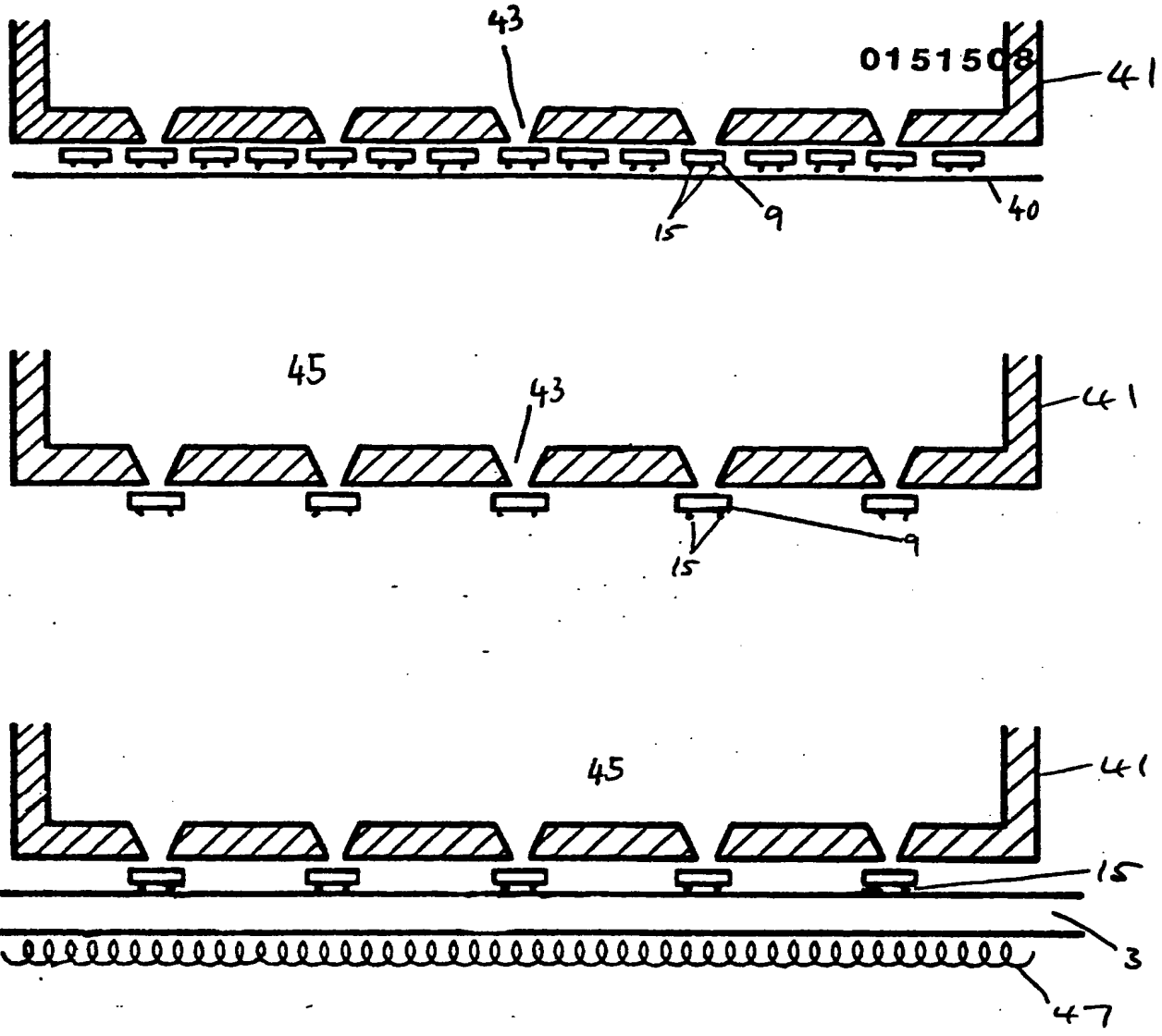

FIGURE 24

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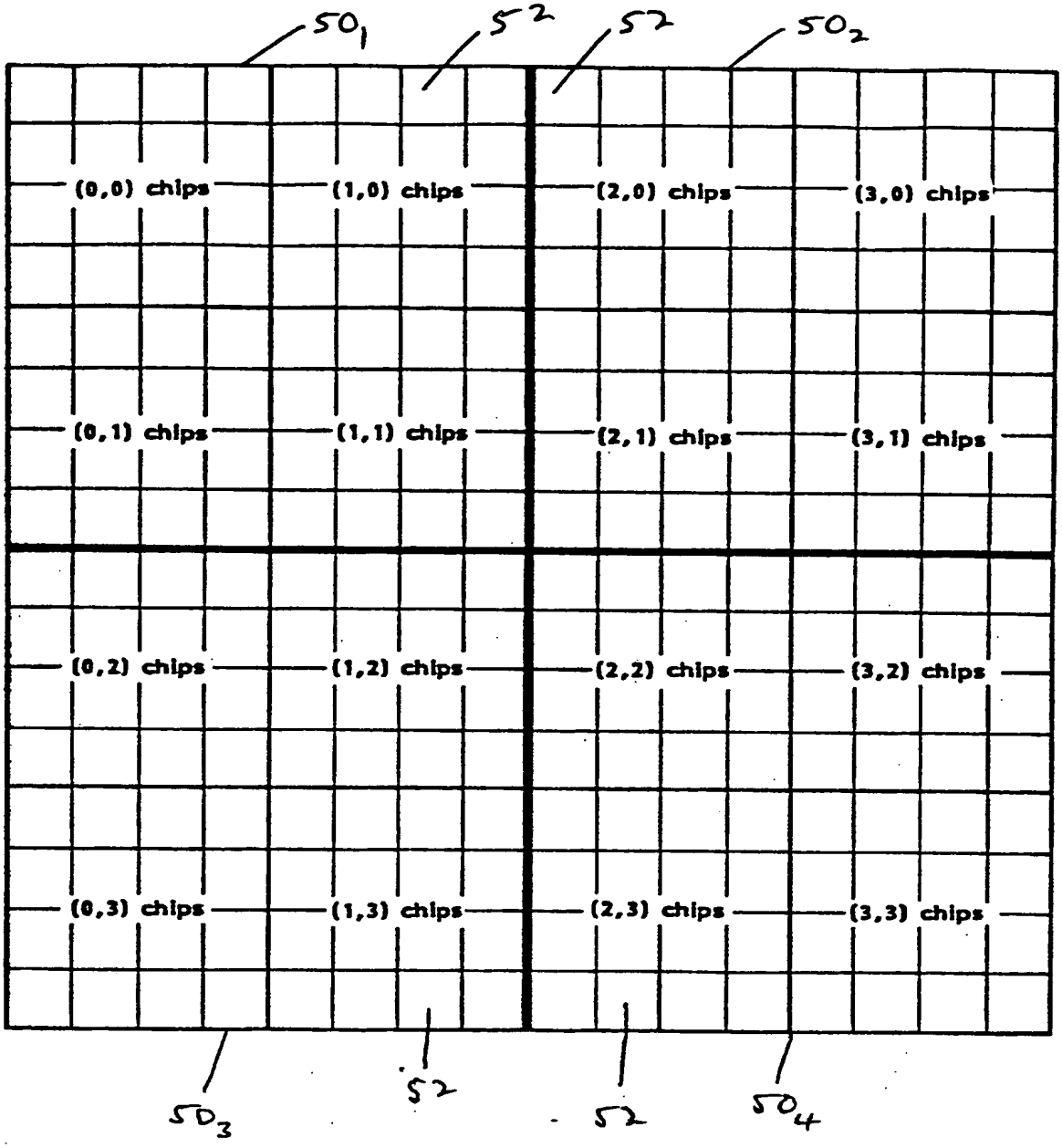

FIGURE 25

FIGURE 26a

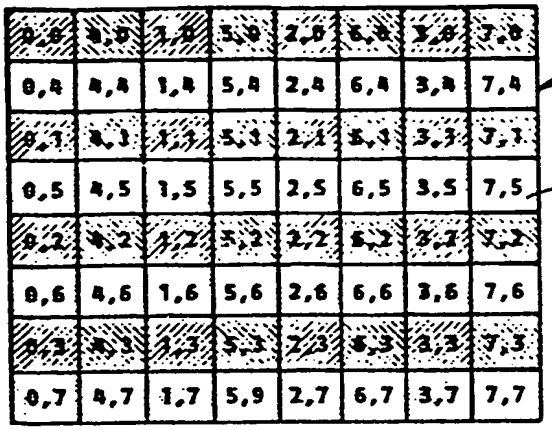

FIGURE 26b

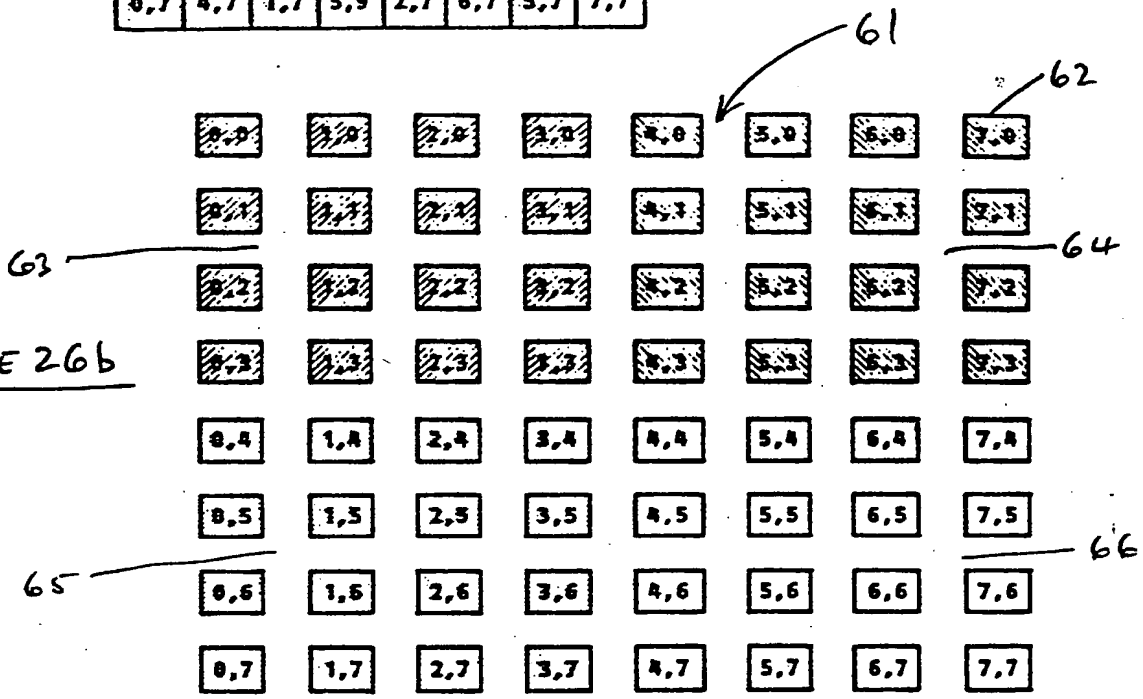

FIGURE 27